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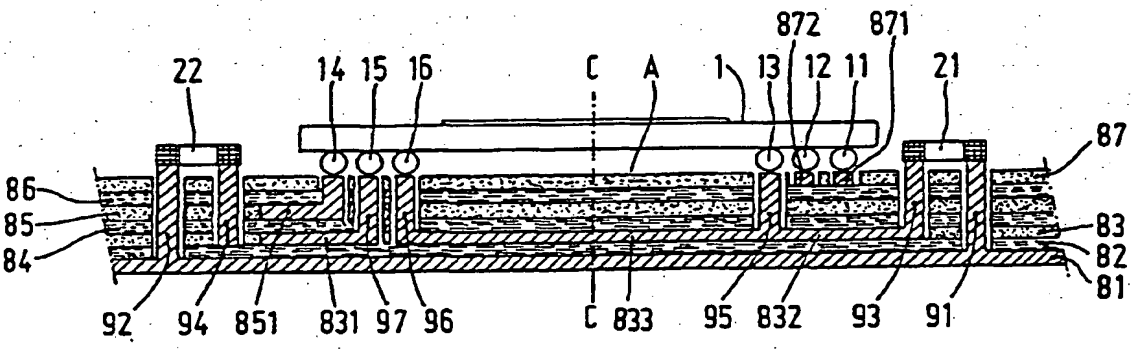
(54) Title: PRINTED CIRCUIT BOARD



(57) Abstract: A printed circuit board intended for mounting at least one integrated circuit (1) and associated decoupling capacitors (21, 22) on the same surface of the printed circuit board. The printed circuit board comprises a stack of alternate conductive and insulating layers (81-87). One of the conductive layers (81) is arranged as a first power plane. The other conductive layers (83, 85, 87) are patterned and provided with signal tracks (831, 851, 871, 872). The stack of layers includes contact holes (91, 92) connected to the first power plane (81), which are arranged for being connected to decoupling capacitors (21, 22). At least one (83) of the patterned conductive layers locally provides at least one second power plane (833) under that part of the aforesaid surface of the printed circuit board which is arranged for mounting an integrated circuit (1) thereon, and furthermore it includes power tracks (832), which form part of connecting means which are arranged for being connected to decoupling capacitors (21, 22) or which make up the connecting means (93, 94). The integrated circuit (1) can be a BGA-type integrated circuit, and the printed circuit board comprising components mounted thereon can be used advantageously in a single-chip cabel modem.

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PRINTED CIRCUIT BOARD

DESCRIPTION

The invention relates to a printed circuit board arranged for mounting at least one integrated circuit and associated decoupling capacitors on the same surface of the printed circuit board, and comprising a stack of alternate conductive and insulating layers, wherein one of the conductive layers is arranged as a first power plane, at least one of the other conductive layers provides a second power plane, and the other conductive layers are patterned and provided with signal tracks, and wherein the stack of layers includes contact holes connected to the first power plane, and connecting means connected to the second power plane, which contact holes and connecting means are arranged for being connected to decoupling capacitors.

A printed circuit board of this type is known from US patent no. 5,068,631.

The power planes of the prior art printed circuit board are comprised of respective conductive layers covering the entire area of the printed circuit board.

Since a power plane comprises the entire conductive layer in question, or, in other words, is a global power plane, the conductive layer cannot provide signal tracks, so that one or more additional conductive layers are required for each power plane, which layers are patterned and provided with signal tracks, as well as a respective associated intermediate insulating layer.

The object of the present invention is to improve the prior art printed circuit board in a manner such that it is not necessary to provide additional global conductive and insulating layers for supply purposes.

In order to accomplish that objective, the invention provides a printed circuit board of the kind referred to in the

introduction, which is characterized in that at least one of the patterned conductive layers locally provides at least one second power plane under that part of the aforesaid surface of the printed circuit board which is arranged for mounting an integrated circuit thereon, and which is furthermore provided with power tracks which at least form part of the connecting means.

It is noted that local power planes are known per se from the prior art printed circuit board, wherein the local power planes are isolated in a global power plane, that is, a power plane which covers the entire area of the printed circuit board. This in contrast to the printed circuit board according to the invention, wherein a local power plane forms part of a conductive layer, which is also provided with a pattern of signal tracks for connecting electric and electronic components.

In a first embodiment of the invention, the first power plane is an earth plane.

In a second embodiment of the invention, the first power plane comprises the conductive layer in question as a whole.

In a third embodiment of the invention, the first power plane is comprised of the conductive layer on the printed circuit board surface positioned opposite the printed circuit board surface that is intended for mounting thereon the at least one integrated circuit and the associated decoupling capacitors.

In a fourth embodiment of the invention, a second power plane comprises part of one of the patterned conductive layers.

In a fifth embodiment of the invention, a second power plane is composed of respective parts of two or more of the patterned conductive layers. In a sixth embodiment, the respective parts are interconnected by contact holes in the stack of layers.

In practice it may be necessary to feed an integrated circuit with different supply voltages, or to feed various integrated circuits each with a different supply voltage.

Accordingly, in a seventh embodiment of the printed circuit board according to the invention, one of the conductive layers or further ones of the conductive layers are arranged as a third power plane or further power planes, wherein the stack of layers includes contact holes connected to the third power plane or further power planes and connecting means connected to a second power plane.

Each local second power plane can be supplied with a different supply voltage via the third power plane or further power planes , if desired, by connecting a respective second power plane to the third power plane and/or to a further power plane.

It will be appreciated that the third power plane and/or the further power planes can be global power planes, which cover substantially the entire area of the printed circuit board.

In an eighth embodiment of the printed circuit board according to the invention, the third power plane or the further power planes comprise part of one or of further ones of the patterned conductive layers. The eighth embodiment of the invention has the advantage that there is no need to provide additional global power planes and the insulating layers associated therewith.

In a ninth embodiment of the printed circuit board according to the invention, the further power planes, which form part of several patterned conductive layers, are mutually arranged in such a manner that the further power planes as a whole cover substantially the entire area of the printed circuit board. Not only is a balanced distribution of conductive material over the printed circuit board as a whole effected in this manner, which is important with a view to preventing warping of the printed circuit board and the like, but furthermore the conductive layers as a whole are shielded from disturbing influences.

In a tenth embodiment of the invention, the connecting means are arranged for connecting a second power plane to one or more of

the third power plane and the further power planes located in different layers. In this manner each second power plane can be provided with a desired supply voltage.

Unlike the printed circuit board that is known from the prior art, wherein the local power planes are to be connected to a global power plane on the same level by means of a so-called π-filter, the invention provides a simple connection by means of power tracks and contact holes of power planes that may be located at different levels. It will be understood that the solution according to the invention obviates the need to use such π-filters, which makes it possible to achieve a greater component density on the same printed circuit board.

If an integrated circuit is to be fed with different supply voltages, it is possible to make advantageous use of the fifth embodiment of the invention as describe above, in which the second power plane is composed of respective parts of two or more of the various patterned conductive layers.

In an eleventh embodiment of the invention, the printed circuit board is arranged for mounting one or more BGA-type integrated circuits thereon. This embodiment allows the use of the printed circuit board in complex, fast electronic circuits, wherein the allowed transmission delay is less than 2 nanoseconds. This makes it possible to use the printed circuit board in a single-chip cable modem.

In a twelfth embodiment of the invention, the connecting means include contact holes in the stack of layers, which are connected to the power tracks or which are arranged for being connected to respective decoupling capacitors.

In a thirteenth embodiment of the invention, the number of power tracks for each second power plane is at least four.

In a fourteenth embodiment of the invention, the dimensions of the second power plane are such that it can be enclosed by a rectangle which circumscribes power pins of an integrated circuit, which is to be

mounted on the printed circuit board that is arranged for that purpose. With a BGA-type integrated circuit, solder balls form the power pins.

The invention will now be explained with reference to the drawing, wherein:

Figures 1 and 2 are schematic, sectional views, not to scale, of printed circuit boards which are presumed to be known, on which a BGA-type of integrated circuit and decoupling capacitors are mounted;

Figure 3 shows, in a similar manner as Figures 1 and 2, an embodiment of the printed circuit board according to the invention, wherein the section is offset parallel to the plane of section to the left and to the right of the dashed line C-C, in order to show both a signal track and a power track beside the local power plane in the same patterned conductive layer;

Figure 4 is a top plan view of important parts of a printed circuit board according to one embodiment of the invention;

Figure 5 is a simulation diagram, showing power tracks; and

Figures 6 and 7 are top plan views of parts of patterned conductive layers comprising a second power plane and further power planes according to the invention.

Figures 1 and 2 each schematically show, not to scale, a part of a prior art printed circuit board in sectional view. Mounted on each of the illustrated printed circuit board parts are an integrated circuit 1 and associated decoupling capacitors, two of which are shown, which are indicated by numerals 21 and 22, respectively. Both in Figure 1 and in Figure 2 the integrated circuit 1 is a BGA-type integrated circuit, with the letters BGA standing for Ball Grid Array. The solder balls that can be seen in Figures 1 and 2 are indicated 11 - 16. The printed circuit boards that are shown in Figures 1 and 2 are arranged, in a manner which is well-known to those skilled in the art, for mounting one or more BGA-type integrated circuits 1 thereon.

The printed circuit board that is shown in Figure 1 is

arranged for mounting at least one integrated circuit 1 and associated decoupling capacitors 21 and 22 on one and the same surface A thereof, and it comprises a stack of alternate conductive and insulating layers 41 - 49, wherein one of the conductive layers, viz. conductive layer 41, is arranged as a first power plane, in this case an earth plane, at least one of the other conductive layers, viz. conductive layer 45, provides a second power plane, and the other conductive layers, viz. conductive layers 43, 47 and 49, are patterned and provided with signal tracks, which are indicated by numerals 431, 471, 472 and 491, respectively.

The stack of layers 41 - 49 is furthermore provided with contact holes 61 and 62, which are connected to first power plane 41, and with connecting means connected to the second power plane, more in particular also contact holes, viz. 63 and 64, wherein contact holes 61 and 63, and 62 and 64 are arranged for being connected to, respectively, decoupling capacitors 21 and 22.

With the prior art printed circuit board of Figure 1, both the first power plane and the second power plane comprise the entire respective conductive layer, in this case conductive layer 41 and conductive layer 45.

Solder balls 13 and 16 are connected to conductive layer 45 by means of contact holes 65 and 66, whilst solder balls 11, 12 and 14 are connected to, respectively, signal tracks 491, 472 and 471, and solder ball 15 is connected to signal track 471 by means of contact holes 67. It will be apparent to those skilled in the art that only a small part of the solder balls and signal tracks shows up in Figure 1.

The printed circuit board that is shown in Figure 2 is arranged for mounting at least one integrated circuit 1 on a surface A and associated decoupling capacitors 21 and 22 on an opposed surface B thereof. Also this printed circuit board includes a stack of alternate conductive and insulating layers 51 - 57, wherein one of the conductive layers, viz. conductive layer 51, is arranged as a first power plane, and

the other conductive layers 53, 55 and 57 are patterned and provided with signal tracks, which are indicated by reference numerals 531, 551, 571 and 572, respectively.

On the one hand decoupling capacitor 21 is directly connected to conductive layer 51 and on the other hand it is connected to solder ball 13 by means of contact hole 71, whilst decoupling capacitor 22 is on the one hand likewise directly connected to conductive layer 51, and on the other hand it is connected to solder ball 16 by means of contact hole 72. Solder balls 11, 12 and 14 are connected to signal tracks 571, 572 and 551, respectively.

The printed circuit board of Figure 2 does not have a second power plane, but power tracks (not shown), since the connections can be sufficiently short, which is not the case with the printed circuit board of Figure 1.

Comparing the printed circuit boards of Figures 1 and 2, the printed circuit board of Figure 1 has the advantage that it is arranged for mounting at least one integrated circuit 1 and associated decoupling capacitors 21 and 22 on one and the same surface A thereof, whilst the printed circuit board of Figure 2 has the advantage that one conductive layer and one insulating layer less will do, because a second power plane is not required. On the other hand, the printed circuit board of Figure 1 has this drawback that it requires a second power plane covering the entire respective conductive layer 45 and the associated insulating layer 46, and the printed circuit board of Figure 2 has this drawback that it is not possible to mount at least one integrated circuit 1 and the associated decoupling capacitors 21 and 22 on one and the same surface thereof.

In other words, from a technical point of view, the printed circuit board of Figure 1 is more desirable, whilst the one of Figure 2 is more advantageous from a commercial point of view.

The printed circuit board proposed in accordance with the

present invention, which is to be described hereafter, combines the advantages of the printed circuit boards of Figures 1 and 2, without having the aforesaid drawbacks thereof. That is, a printed circuit board that is technically most desirable and commercially most advantageous is provided.

The printed circuit board that is shown in Figure 3 is arranged for mounting at least one integrated circuit 1 and associated decoupling capacitors 21 and 22 on one and the same surface thereof, and it includes a stack of alternate conductive and insulating layers 81 - 87, wherein one of the conductive layers, conductive layer 81, is arranged as a first power plane, one of the other conductive layers, layer 83, provides a second power plane, and the other conductive layers 85 and 87 are patterned and provided with signal tracks 851, and 871 and 872, respectively. The stack of layers 81 - 87 includes contact holes 91 and 92, which are connected to the first power plane 81, and connecting means connected to the second power plane, which comprise contact holes 93 and 94 as well as power tracks, only one of which power tracks is shown in Figure 3 and indicated by numeral 832, whilst it is noted that the part of Figure 3 to the right of line CC is offset parallel to the part shown to the left of line CC, so as to be able to show both signal track 831 and power track 832, whereas either two signal tracks 831 or two power tracks 832 would show up without this offset. The contact holes 91 and 92 and the connecting means (contact holes 93 and 94 and power track 832) are arranged for connection to decoupling capacitors 21 and 22.

It is a characteristic feature of the printed circuit board of Figure 3 that one of the patterned conductive layers, conductive layer 83 in this case, locally provides the second power plane 833 under that part of surface A of the printed circuit board which is arranged for mounting integrated circuit 1 thereon, and that the layer is furthermore provided with power tracks 832, which form part of the connecting means.

Thus, the invention provides a local power plane 833 and power tracks 832 as elements of a patterned conductive layer 83 and providing signal tracks 831, rather than the global conductive layer 45 of the printed circuit board of Figure 1, which does not form part of a pattern and which is not provided with signal tracks, whilst it is possible, in contrast to the printed circuit board of Figure 2, to mount components on one and the same surface.

In other words, whilst the printed circuit board of Figure 1 requires a global second power plane, which makes it necessary to provide an additional conductive layer and an additional insulating layer, the printed circuit board of Figure 2 only requires power tracks and not a second power plane, although it is not possible to mount the components on one and the same surface thereof; with the printed circuit board according to Figure 3, on the contrary, it is possible to mount the components on one and the same surface thereof, whilst a local second power plane and signal tracks are provided, albeit as part of a patterned conductive layer and provided with signal tracks, as a result of which the provision of an additional conductive layer and an associated additional insulating layer is not necessary.

If the conductive layer 83 that provides the local second power plane 833 also provides the surface A of the printed circuit board that is arranged for mounting an integrated circuit 1 thereon, the connecting means consist of power tracks 832, because contact holes 93 and 94 are not required in that case.

Figure 4 schematically shows in top plan view the relative positions and/or connections of a BGA-type integrated circuit 1, decoupling capacitors 2? and local power plane 833 provided with power tracks 834. A few of the illustrated solder balls are indicated by numeral 17, and a few contact holes are indicated by numeral 98, which contact holes 98 are used for out-fanning of signal lines, which is possible according to the invention in that the second power plane is

interrupted at the location of contact holes 98. Thanks to the local power plane 833 including multiple power tracks 834 for connection with capacitors 834 near integrated circuit 1, a solid power distribution is provided all the same. The voltage across decoupling capacitors 23 is stable in relation to the earth plane (81 in Figure 3). Since the power tracks 834 to the local power plane 833 are short, the electromagnetic field that is generated is only small, so that the voltage will be stable. Also the fact that only a small electromagnetic field can be generated within the local power plane 833 ensures an optimum distribution of power to the various power solder balls of solder balls 17.

The local power plane 833 must not necessarily be a massive layer of copper, but it may consist of a meshwork, for example. Furthermore it is not necessary for the local power plane 833 to be comprised of a single conductive layer, but a number of conductive layers may provide a number of local sub-power planes, which are interconnected by means of respective contact holes so as to form one local power plane.

Figure 6 shows in top plan view a part of a patterned conductive layer, for example layer 83, comprising a second power plane 832. In the illustrated embodiment, layer 83 comprises a third power plane 100.

Figure 7 is a top plan view of a part of a further patterned conductive layer 110 comprising a second power plane 115 and one further power plane 120.

In accordance with the invention, the third power plane 100, for example, can provide a supply voltage of for example 2.5 V, and the further power plane 120 can provide a supply voltage of for example 3.3 V.

By connecting the second power plane 832 to the further power plane 120 via respective contact holes and connecting means, the second power plane 832 can be connected to a voltage of 3.3 V. On the

other hand, the second power plane 115 can be connected to the third power plane 100, likewise via contact holes and connecting means, as a result of which second power plane 115 can be fed with a voltage of 2.5 V. Also other voltages are possible, of course.

Third power plane 100 and further power plane 120 are preferably positioned in such a manner with respect to each other that they cover the entire printed circuit as a whole. This provides a very good shielding effect, whilst warping of the printed circuit board is prevented as much as possible.

It will be apparent that an integrated circuit can be provided with different supply voltages by dividing the second power plane and connecting it to different power planes, via respective contact holes and connecting means.

Unlike the aforesaid US patent, it is not necessary to use π-filters or other connection components in the printed circuit board according to the invention, since the second power plane and the power planes to which the second power plane is to be connected via the respective contact holes and connecting means extend over various layers of the printed circuit board.

It will be apparent that the use of global power planes is avoided as much as possible with the printed circuit board according to the invention, which makes it possible to minimize the number of layers of the printed circuit board, which is clearly advantageous from an economic viewpoint.

Figure 4 shows seven decoupling capacitors 23 and respective power tracks 834, but also a lower number will be capable of providing the advantageous effects of the present invention. It may be advantageous to use four or more power tracks 834.

The influence of the number of power tracks 834, the resistance of each power track 834 and the inductance of the power tracks 834 are illustrated in the simulation diagram of Figure 5, wherein the X-

axis indicates the number of power tracks 834 and the Y-axis indicates the amount of noise caused by dynamic power consumption of the integrated circuit 1. The standard curve represents a standard situation with a varying number of power tracks 834. The greatest differences are found when only a small number of 1 - 3 power tracks 834 are used. The 2*R-curve shows the situation wherein the power tracks 834 exhibit twice the resistance of the power tracks 834 of the standard curve. The 2*L-curve shows the situation wherein the power tracks 834 exhibit twice the inductance of the power tracks 834 of the standard curve. It is apparent from the curves that inductance is more important than resistance, whereby it is noted that thinner tracks exhibit a greater resistance and that longer tracks exhibit a higher inductance. As can be expected, it is preferable to use short power tracks 834, therefore.

A mechanical analogon of the local power plane 833 with power tracks 834 connected to decoupling capacitors 23 is a trampoline. All the available knowledge of trampolines can thus be translated to the local power plane by a person skilled in the art.

The invention is not limited to BGA-type integrated circuits, but it can also be used with, for example, QFP-type integrated circuits, the letters QFP standing for Quad Flat Package, as well as with other types of integrated circuits.

The dimensions of the local second power plane can be such that the second power plane can be enclosed by a rectangle which circumscribes power pins of an integrated circuit, which is to be mounted on the printed circuit board that is arranged for that purpose.

The printed circuit board according to the invention can be used advantageously in a single-chip cable modem and in other electronic apparatus.

CLAIMS

1. A printed circuit board arranged for mounting at least one integrated circuit and associated decoupling capacitors on the same surface of said printed circuit board, and comprising a stack of alternate conductive and insulating layers, wherein one of said conductive layers is arranged as a first power plane, at least one of the other conductive layers provides a second power plane, and the other conductive layers are patterned and provided with signal tracks, and wherein said stack of layers includes contact holes connected to said first power plane, and connecting means connected to said second power plane, which contact holes and connecting means are arranged for being connected to decoupling capacitors, characterized in that at least one of said patterned conductive layers locally provides at least one second power plane under that part of said surface of said printed circuit board which is arranged for mounting an integrated circuit thereon, and which is furthermore provided with power tracks which at least form part of said connecting means.

2. A printed circuit board according to claim 1, characterized in that said first power plane is an earth plane.

3. A printed circuit board according to claim 1 or 2, characterized in that said first power plane comprises said conductive layer as a whole.

4. A printed circuit board according to any of the preceding claims, characterized in that said first power plane is comprised of the conductive layer on the printed circuit board surface positioned opposite said printed circuit board surface that is intended for mounting thereon said at least one integrated circuit and said associated decoupling capacitors.

5. A printed circuit board according to any of the preceding claims, characterized in that a second power plane comprises part of one

of the patterned conductive layers.

6. A printed circuit board according to any of the claims 1 - 4, characterized in that a second power plane is composed of respective parts of two or more of the patterned conductive layers.

7. A printed circuit board according to claim 6, characterized in that the respective parts are interconnected by contact holes in the stack of layers.

8. A printed circuit board according to any of the preceding claims, characterized in that one of said conductive layers or further ones of said conductive layers are arranged as a third power plane or further power planes, wherein said stack of layers includes contact holes connected to said third power plane or further power planes and connecting means connected to a second power plane.

9. A printed circuit board according to claim 8, characterized in that said third power plane or said further power planes comprise part of one or of further ones of the patterned conductive layers.

10. A printed circuit board according to claim 8, characterized in that said further power planes, which form part of different patterned conductive layers, are mutually arranged in such a manner that said further power planes as a whole cover substantially the entire area of the printed circuit board.

11. A printed circuit board according to claim 8, 9 or 10, characterized in that said connecting means are arranged for connecting a second power plane to one or more of said third power plane and said further power planes.

12. A printed circuit board according to any of the preceding claims, characterized in that said printed circuit board is arranged for mounting one or more BGA-type integrated circuits thereon.

13. A printed circuit board according to any of the preceding claims, characterized in that the connecting means include contact holes in the stack of layers, which are connected to the power tracks or which

are arranged for being connected to respective decoupling capacitors.

14. A printed circuit board according to any of the preceding claims, characterized in that the number of power tracks for each second power plane is at least four.

15. A printed circuit board according to any of the preceding claims, characterized in that the dimensions of the second power plane are such that it can be enclosed by a rectangle which circumscribes power pins of an integrated circuit, which is to be mounted on the printed circuit board that is arranged for that purpose.

16. A printed circuit comprising components mounted thereon according to any of the preceding claims.

17. A method for mounting components on a printed circuit board, characterized in that a printed circuit board according to any of the claims 1 - 15 is used.

18. Electronic apparatus, characterized in that said apparatus is fitted with a printed circuit board comprising components mounted thereon according to claim 16.

19. Electronic apparatus according to claim 16, characterized in that said apparatus is a modem.

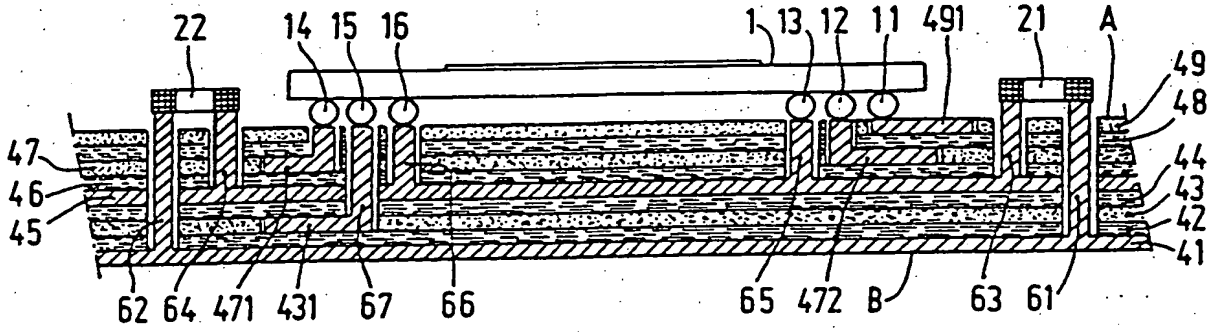

FIG. 1

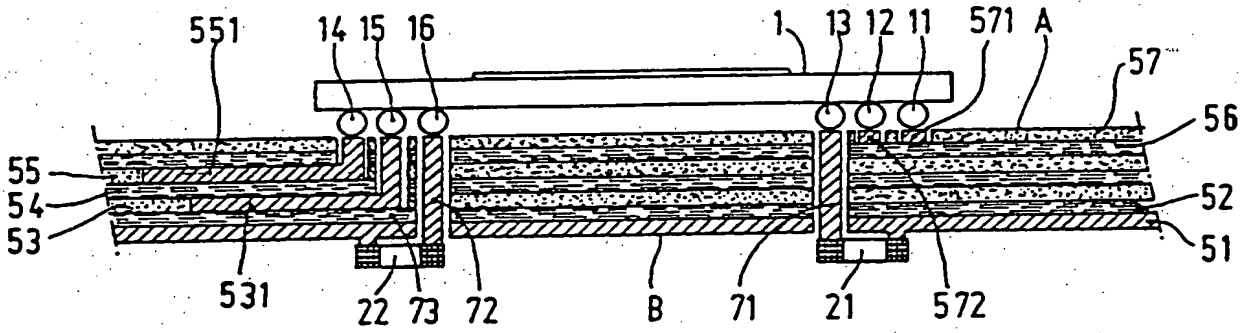

FIG. 2

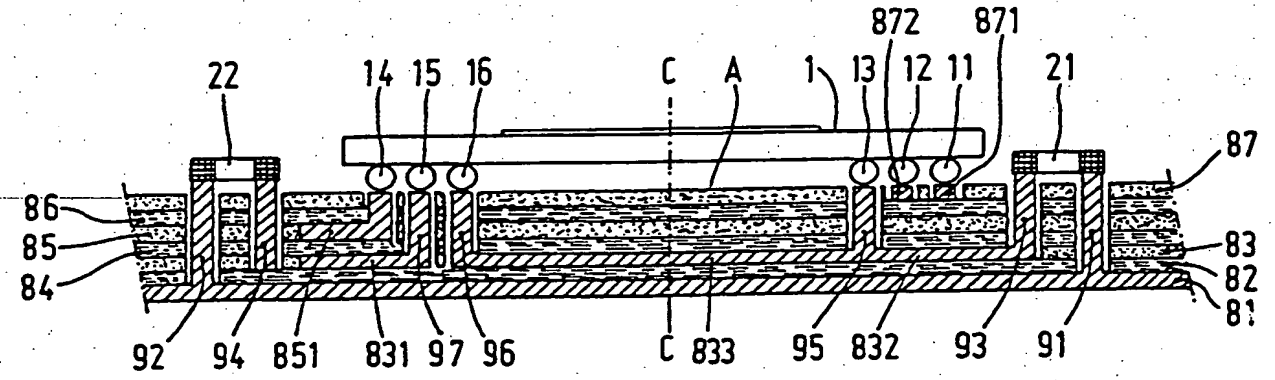

FIG. 3

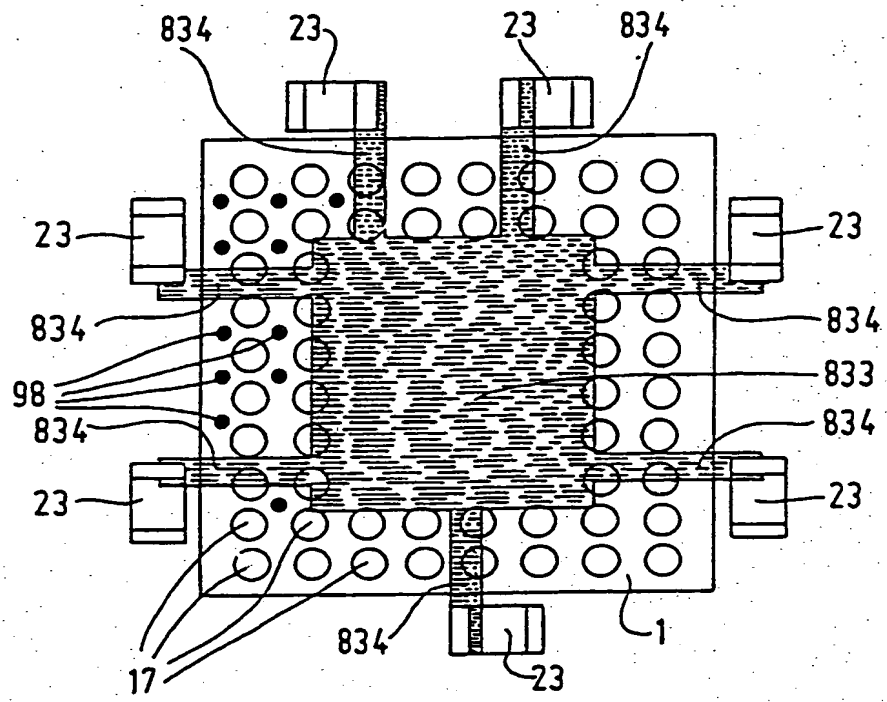

FIG. 4

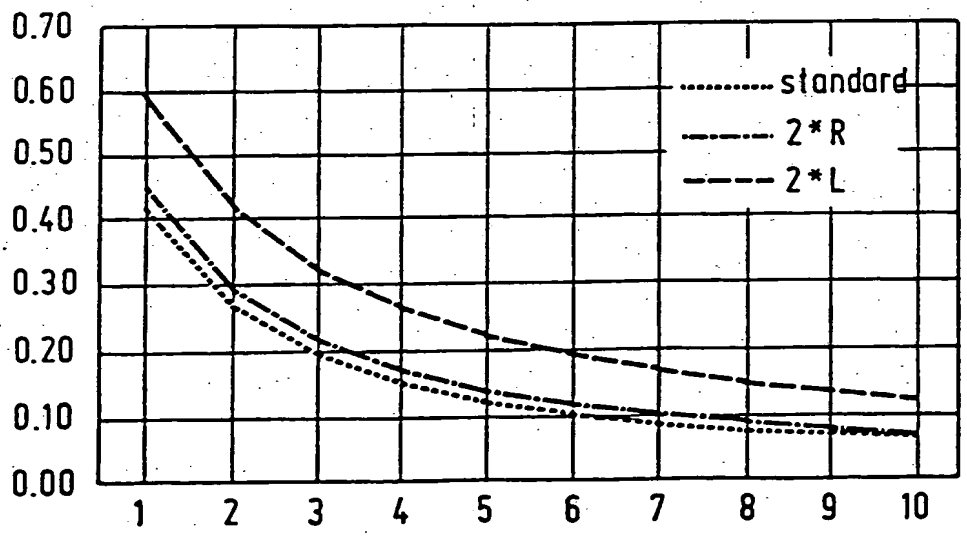

FIG. 5

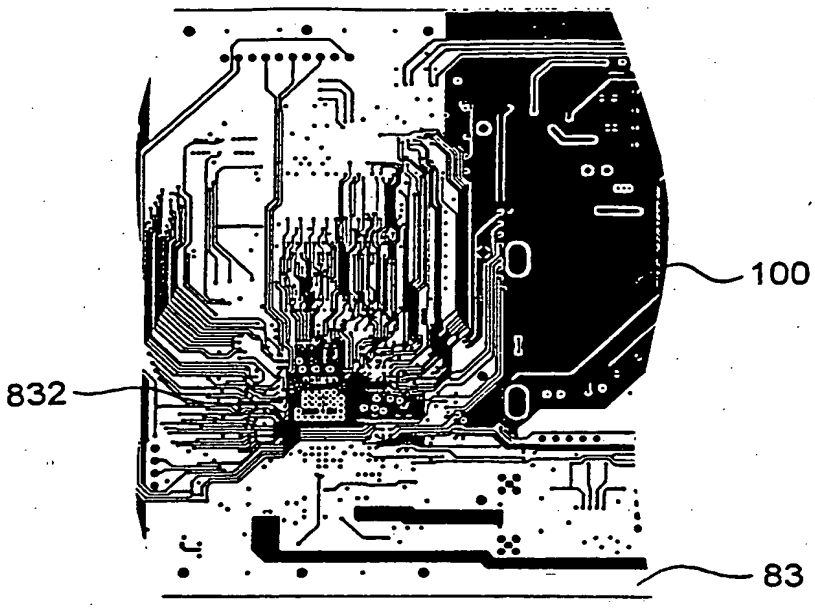

FIG. 6

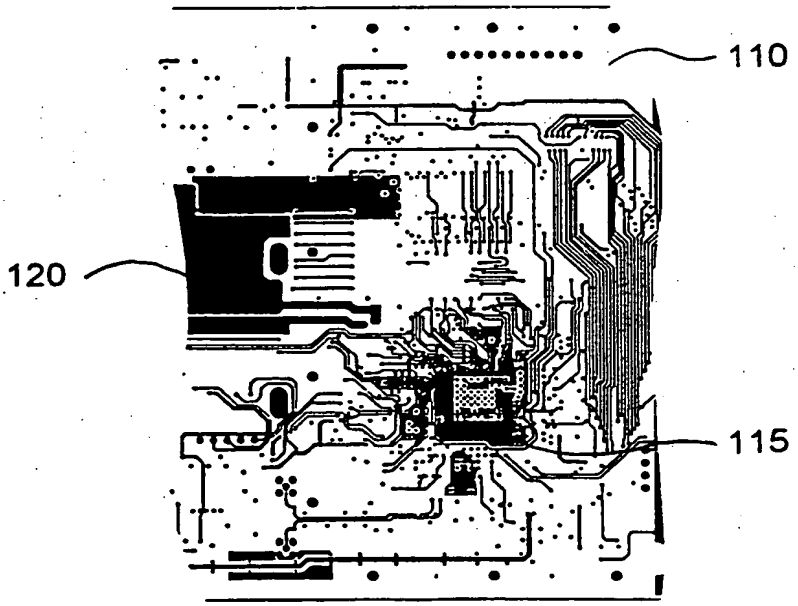

FIG. 7

INTERNATIONAL SEARCH REPORT

Inten al Application No
PCT/NL 01/00057

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K1/02 H05K1/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 068 631 A (VINCE RICHARD A) 26 November 1991 (1991-11-26) cited in the application abstract; figures	1-5, 15-17
A	EP 0 873 046 A (FUJI XEROX CO LTD) 21 October 1998 (1998-10-21) abstract; figures	1-3,16, 17
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 08, 30 June 1999 (1999-06-30) & JP 11 087880 A (OKI ELECTRIC IND CO LTD), 30 March 1999 (1999-03-30) abstract	1-5,16, 17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 May 2001	01/06/2001

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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